REMARKS

The above-identified patent application has been amended prior to examination. No new matter was added.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: January 28, 2003

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Version with markings to show changes made

In the specification:

Paragraph beginning at page 1, line 21 has been amended as follows:

--One or more of the following features may also be included. Each of the blocks includes [at least one input signal port and] at least one output signal port. [The] A plurality of input signal values and the output signal values have at least one attribute. The attribute may be a name, a data type, a numeric value and/or a dimensionality. The ordered set is a linked list data structure. The linked list data structure is a tree data structure, the tree data structure including m + n nodes. [M] m represents a number of independent signals and n represents a number of composite signals.--

Paragraph beginning at page 2, line 15 has been amended as follows:

--According to another aspect of the invention, a block diagram modeling process includes providing a first block and a second block, the blocks representing functional entities [that operate on a plurality of input signal values], generating a plurality of output signal values from the first and second block, grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal and processing the composite signal in a third block.--

Paragraph beginning at page 2, line 26 has been amended as follows:

--The process further includes decomposing the composite signal into [the] a plurality of input signal values.--

Paragraph beginning at page 3, line 6 has been amended as follows:

--In another aspect, the invention features a computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to provide a plurality of blocks, each of the blocks representing functional entities [that operate on a plurality of input signal values], generate a plurality of output signal values from the plurality of blocks, group the plurality of output

signal values as an ordered set in a multiplexer as a first composite signal and output the first composite signal.--

Paragraph beginning at page 3, line 20 has been amended as follows:

--In another aspect, the invention features a processor and a memory configured to provide a plurality of blocks, each of the blocks representing functional entities [that operate on a plurality of input signal values], generate a plurality of output signal values from the plurality of blocks, group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal and output the first composite signal.--

Paragraph beginning at page 10, line 3 has been amended as follows:

--Referring to FIG. 4, a tree structure 76 is shown illustrating one representation of the two composite signals c_1 and c_2. The tree data structure 76 contains five nodes [(shown as black dots)], one node for each signal, i.e., s_1, s_2, s_3, c_1 and c_2. The link between two signals, represented by an arrowhead line, indicates a grouping relationship. Specifically, the four links (i.e., arrowhead lines) coming from composite signal c_2 indicate a grouping of four signals in composite signal c_2 while the two links coming from composite signal c_1 indicate a grouping of two signals in composite signal c_1. The link from composite signal c_2 to single signal s_1 indicates that composite signal c_2 contains single signal s_1. Likewise, the two links from composite signal c_2 to single signal s_2 indicate that composite signal c_2 contains two s_2 single signals. The link from composite signal c_2 to composite signal c_1 indicates the composite signal c_2 also includes composite signal c_1. Completing the example, the link from composite signal c_1 to single signal s_2 indicates that composite signal c_1 includes single signal s_2 and the link from composite signal c_1 to single signal s_3 indicates that composite signal c_1 also includes single signal s_3. The links are ordered left to right using black dots to preserve signal orders in the composite signals. Thus, the order of the black dots under composite signal c_2 indicates that its constituent signals are ordered as single signal s_1, single signal s_2, single signal s_2 and composite signal c_1. The order of black dots under composite signal c_1 indicates that its constituent signals are ordered as single signal s_3 and single signal s_2.--

29. (Amended) A modeling process comprising:

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providing a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signals;

grouping the output signals as an ordered set in a multiplexer as a composite signal; and

outputting the composite signal.

33. (Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

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provide a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.

34. (Amended) A processor and memory configured to

provide a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.

In the claims:

Amend claims 1, 2, 3, 14, 16, 21, 25, 29, 33 and 24 as follows:

1. (Amended) A modeling process comprising:

providing a plurality of blocks, each of the blocks representing functional entities [that operate on a plurality of input signal values];

generating a plurality of output signal values from the plurality of blocks;

grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

outputting the first composite signal.

2. (Amended) The process of claim 1 wherein each of the blocks includes [at least one input signal port and] at least one output signal port.

3. (Amended) The process of claim 1 wherein [the] a plurality of input signal values and the output signal values have at least one attribute.

14. (Amended) A block diagram modeling process comprising:

providing a first block and a second block, the blocks representing functional entities [that operate on a plurality of input signal values];

generating a plurality of output signal values from the first and second block;

grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

processing the composite signal in a third block.

16. (Amended) The process of claim 14 wherein [at least one of the] an input [signals] signal is a second composite signal.

17. (Amended) The process of claim 14 further comprising decomposing the composite signal into [the] a plurality of input signal values.

21. (Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

provide a plurality of blocks, each of the blocks representing functional entities [that operate on a plurality of input signal values];

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.

25. (Amended) A processor and a memory configured to:

provide a plurality of blocks, each of the blocks representing functional entities [that operate on a plurality of input signal values];

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.

29. (Amended) A modeling process comprising:

providing a plurality of blocks, each of the blocks representing a functional entity that [operates on one or more input signal values and] generates one or more output signals;

grouping the output signals [use] as an ordered set in a multiplexer as a composite signal; and

outputting the composite signal.

33. (Amended) A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

provide a plurality of blocks, each of the blocks representing a functional entity that [operates on one or more input signal values and] generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.

34. (Amended) A processor and memory configured to

provide a plurality of blocks, each of the blocks representing a functional entity that [operates on one or more input signal values and] generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.